cameleon

FPGA smart camera family

Product Brief v1.6

Cameleon is Fast-adaptive, has flexible imaging and stereoscopic view

Cameleon is an innovative USB2.0 camera based on FPGA system-on-chip (SOC) technology. The camera with a powerful HSDK (hardware-software development kit) opens ways for rapid customization and integration of various digital systems into camera itself. The camera is a ready made solution, but still open for a user to add his own features if he wishes so.

The true power of FPGA (Field-Programmable Gate Array) over the sequential microprocessor is a pipelined parallel data processing. Parallelism reduces system clock and power consumption considerably while boosting processing power. With the latest set of tools from Xilinx (System Generator and Accel DSP) you can rapidly develop DSP algorithms even in MathWorks MATLAB (example included).

The camera is sold in two basic configurations: MONO (single sensor) or STEREO (dual sensors). You can upgrade your camera any time by purchasing additional sensor head. Up to 2 additional heads can be mounted to a single baseboard. The images from multiple sensors are pixel synchronous.

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Camera structure

The camera is composed of three basic parts:

- FPGA System on a module
- Base Sensor board
- Head sensor board

All of the vital system components are assembled on a module (Figure 2 right). This includes power supply, FPGA, DDR SDRAM, USB controller and SPI Flash (Figure 1). The module is USB powered with triple DC-DC converters for maximal power efficiency (SMPS - Switching Mode Power Supply in Figure 1). The core is a Xilinx Spartan3E or Spartan6 FPGA with DDR or DDR3 SDRAM. The DDR3 has 16-bit wide data bus running at 800 Mbps offering 1600 MB/s peak bandwidth. The gateway to the PC is a well proven Cypress CY7C68013A (also known as FX2) USB microcontroller which offers up to 36 MB/s of bandwidth from FPGA to PC.
The board also includes non-volatile SPI FLASH memory. The SPI bus is shared by FPGA and FX2 which is necessary to enable USB firmware upgrade and FPGA booting. The system board is connected to the base board through two shock-proof 80-pin connectors. The power and IO signals are routed to on-board sensor and external connectors - head and expansion connector.

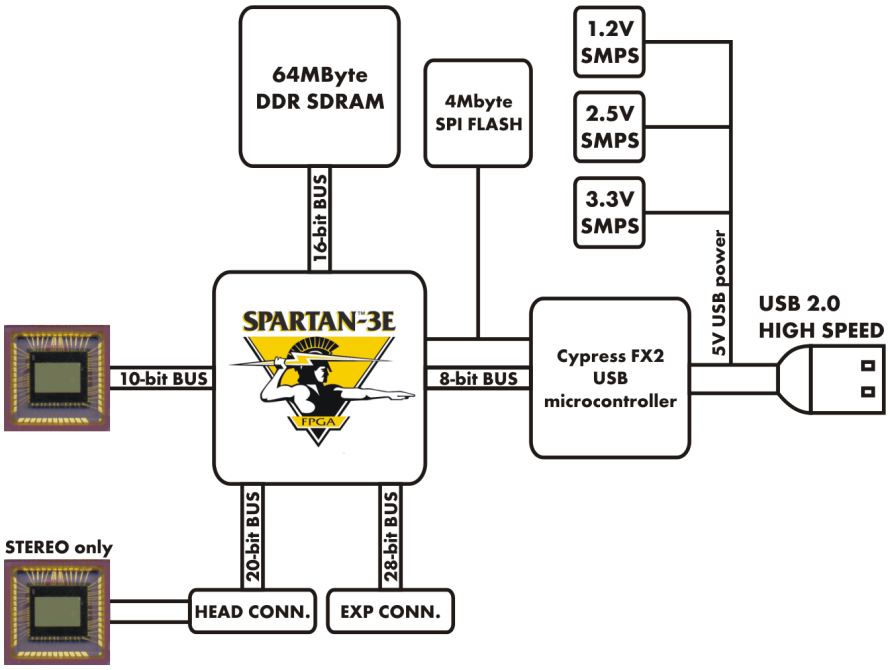
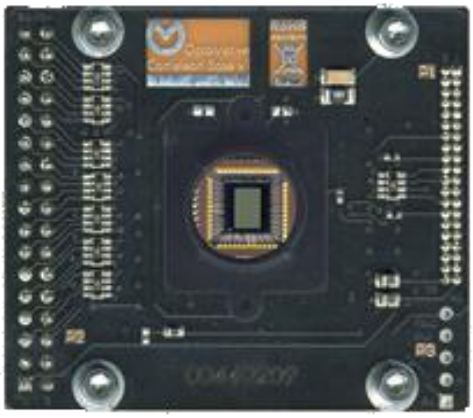
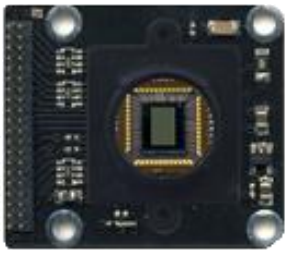


Figure 1: Camera structure block scheme

The camera baseboard and head use Aptina VWGA 1/3"CMOS imaging sensor with a global shutter. The baseboard is offered also with also with 1.3 mega pixel Monochrome or 3 mega pixel 1/2" rolling shutter sensor. Global shutter means that exposure of all pixels starts and stops at the same time preventing motion blur for fast moving objects.





Sensor head

Base board connectors:

- Mini USB B
- 6-pin 2.54 mm JTAG header for FPGA programming and debug
- 6-pin 2.54 mm SPI header for direct FLASH programming
- 5-pin 2.54 mm header for industrial (IP68) USB connector
- 40-pin dual row 1.27 mm header for head attachment
- 34-pin dual row 2.54 mm expansion header

The head is attached to the base board using a 40-pin ribbon cable. There are different lengths available for user to choose from (up to 1 m). The cable has 3.3V and 5V power and 20 IO signals (3.3V LVCMOS).

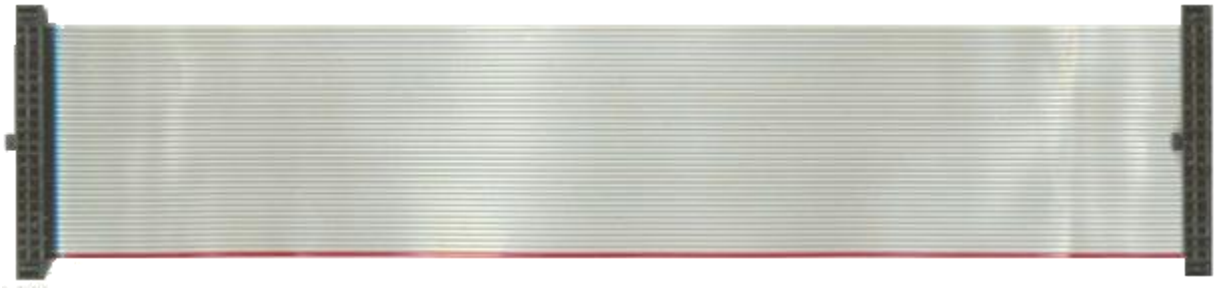


Figure 2: Camera head ribbon cable

Soft hardware concept

As stated, the FPGA itself has no architecture and is blank by default. When properly programmed it becomes the "brains" of the camera. We have to define system architecture to achieve that. The system was composed using Xilinx Embedded Development Kit (EDK). Basically it is an embedded system with a MicroBlaze 32-bit soft microprocessor. The MicroBlaze is used to initialize and to setup the system. The horsepower for high bandwidth data streaming is a Multiport Memory Controller (MPMC).

Using a custom built DMA engine (XPS_NPI_DMA) it can stream data from multiple imaging sensors to external RAM. The processed data is buffered inside DDR SDRAM and send to USB through XPS_FX2. When transferring raw image to USB the data is transferred directly from DMA engine to XPS_FX2 for highest bandwidth utilization. The XPS_I2C_SLAVE is used to send commands from the PC to the MicroBlaze - low speed communication. The XPS_I2C peripheral is used to communicate with imaging sensors. It has the ability to send commands to multiple sensors at the same time (also on external sync signal). Standard EDK cores are used to communicate with RS232 (XPS_UARTLITE), SPI FLASH (XPS_SPI)…

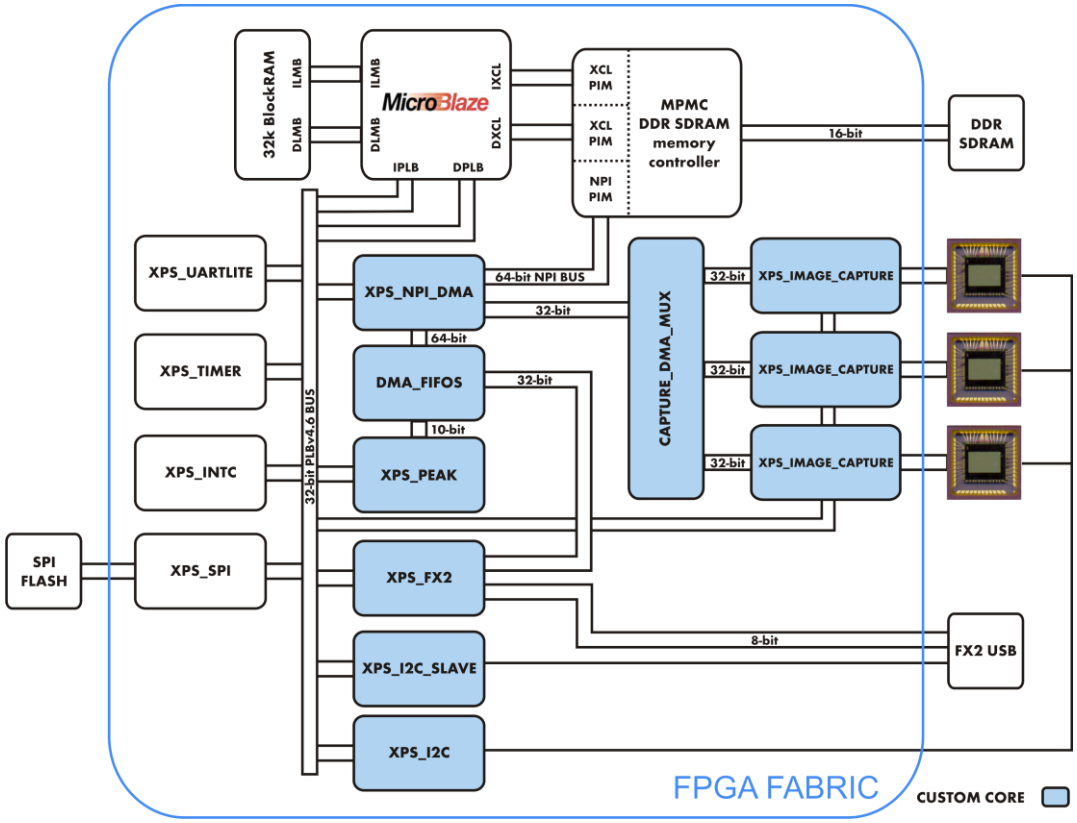


Figure 3: FPGA system-on-chip architecture

Key camera features:

- Industrial vision proven CMOS Aptina sensors from VGA to 3 mega pixel
- Up to 3 sensors per one camera perfectly synchronized
- Can capture video or processed information
- Image processing inside the camera
- Large Xilinx Spartan 3E or Spartan 6 FPGA
- 64MB DDR SDRAM or 128MB DDR3 SDRAM in-camera buffer
- USB powered
- 48 additional IO pins for expansion and user programming
- Multiple cameras can be synchronized to an external trigger or to a master camera (strobe)
- Firmware (soft-hw and sw) can be upgraded in a minute
- Full source code of the complete system simplifies integration and enables user to customize the camera to his needs or to train FPGA SoC designing (research and development)

Targeted to:

- Industrial process automation
- Medical devices
- 3D applications
- Institutes and Universities for research and development
- General R&D in Embedded Vision

Specification table

Camera Family		Cameleon		
Camera model		WVGA	1.3MEGA	3MEGA
Imaging sensor	Model (Aptina)	MT9V034	MT9M001	MT9T031
	Sensor type (CMOS)	global shutter	rolling shutter, global reset	rolling shutter, global reset
	Colour filter	mono or Bayer	mono	Bayer only
	Optical format	1/3"	1/2"	1/2"
	Active pixels	752 x 480	1280x1024	2048x1536
	Region of interest	YES	YES	YES
	Pixel size	6.0 x 6.0 µm	5.2 x 5.2 µm	3.2 x 3.2 µm
	Pixel clock speed	27 MHz	48 MHz	48 MHz
	Frame rate (full resolution)*	63 FPS	30 FPS	13 FPS
	ADC resolution	10 bit	10 bit	10 bit
	Responsivity	4.8 V/lux-sec	2.1 V/lux-sec	>1 V/lux-sec
	Dynamic range	55dB linear 110dB HDR	61dB	68dB
	Auto Exposure	YES	NO	NO
	Gain (Digital or Analogue)	YES	NO	NO
FPGA module	FPGA type	Xilinx Spartan 3E 1600 or Xilinx Spartan 6LX 45 or Xilinx Spartan 6LX 75		
	DDR SDRAM (or Volatile memory)	64MB, 16bit, 100MHz or 128MB, 16bit, 400MHz DDR3		
	Non-volatile memory	4MB or 8MB flash		
	USB	BULK High speed up to 36 MB/s		
Camera base	Size (including lens mount)	47 x 54 x 30 mm		
	Mass (including lens mount)	37g		
	Trigger modes	Free running Snapshot on trigger Sync and start on trigger		
	Power consumption at 5V USB supply	Mono 310 mA Stereo 350 mA		
Head	Size (including lens mount)	30 x 35 x 18 mm		
	Mass (including lens mount)	7 g		
	Cable length	Up to 1m		
Electrical	Input voltage	5V USB, or external 5V		
	Consumption	Up to 6W with external power		
	IO	48 x bidirectional LVCMOS from FPGA		
	IO isolation	1x input, 1x output with ISO board		
	USB	High Speed BULK up to 36 Mb/s		

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Mechanical	Lens mount	M12 (lens included) or C- / CS-mount (1" 32G thread, lens not included)
	Temp range	0 - 50°C
	Protection	Up to IP67 with housing
	Housing material	CNC-machined aluminium, anodized in a special OptoMotive blue colour
	RoHS	RoHS compliant
	Fixing holes	4 x M2.5 OEM / 1 x M6 with housing
Functionalities	On-board image processing	As an option (if an IP Core is integrated)
	IP cores	Yes. Can be implemented into the camera additionally. See the List of IP Cores available.
	Open reference design	Yes
	Open architecture	Yes
	Software	Compatible with OptoMotive SHARKi software (full source included)
	Operating system	Windows 7, 64bit or 32bit
	Development tools	Xilinx EDK version 13.3 or later. For IP core development VHDL or System Generator /MATLAB Simulink or other RTL design tool
Standards	CE	EN55022, class A EN61000-4-2 EN61000-4-3 EN61000-4-4 EN61000-4-6
	FCC	Part 15, class A
	RoHS	Compliancy as per European directive 2002/95/EC

Table 1: Specifications

*This is sensor maximal frame rate. USB data rate limits streaming video frame rate.

Each camera is supplied with:

- Software: SHARKi software for image capturing and recording
- Cable: USB 2.0 cable 1.8 m length

Specification: Resolution / FPS

Specifications of resolutions and maximum frame rates:

Sensor type	WVGA	1.3MEGA	3MEGA
Active pixels	752 x 480	1280 x 1024	2048 x 1536

STANDARD RESOLUTIONS

Resolution	Active pixels	MAX. FRAME RATE	MAX. FRAME RATE	MAX. FRAME RATE
Full frame 0.3M		63 FPS	N/A	N/A
Full frame 1.3M		N/A	30 FPS	N/A
Full frame 3M		N/A	N/A	13 FPS
2K	2048 x 1080	N/A	N/A	19 FPS
HD 1080	1920 x 1080	N/A	N/A	19 FPS
XGA	1024 x 768	N/A	N/A	26 FPS
HD 720	1280 x 720	N/A	42 FPS	28 FPS
SVGA	800 x 600	N/A	50 FPS	34 FPS
PAL	768 x 576	N/A	53 FPS	35 FPS
WVGA	752 x 480	63 FPS	63 FPS	42 FPS
VGA	640 x 480	63 FPS	63 FPS	42 FPS
QVGA	320 x 240	116 FPS	122 FPS	81 FPS

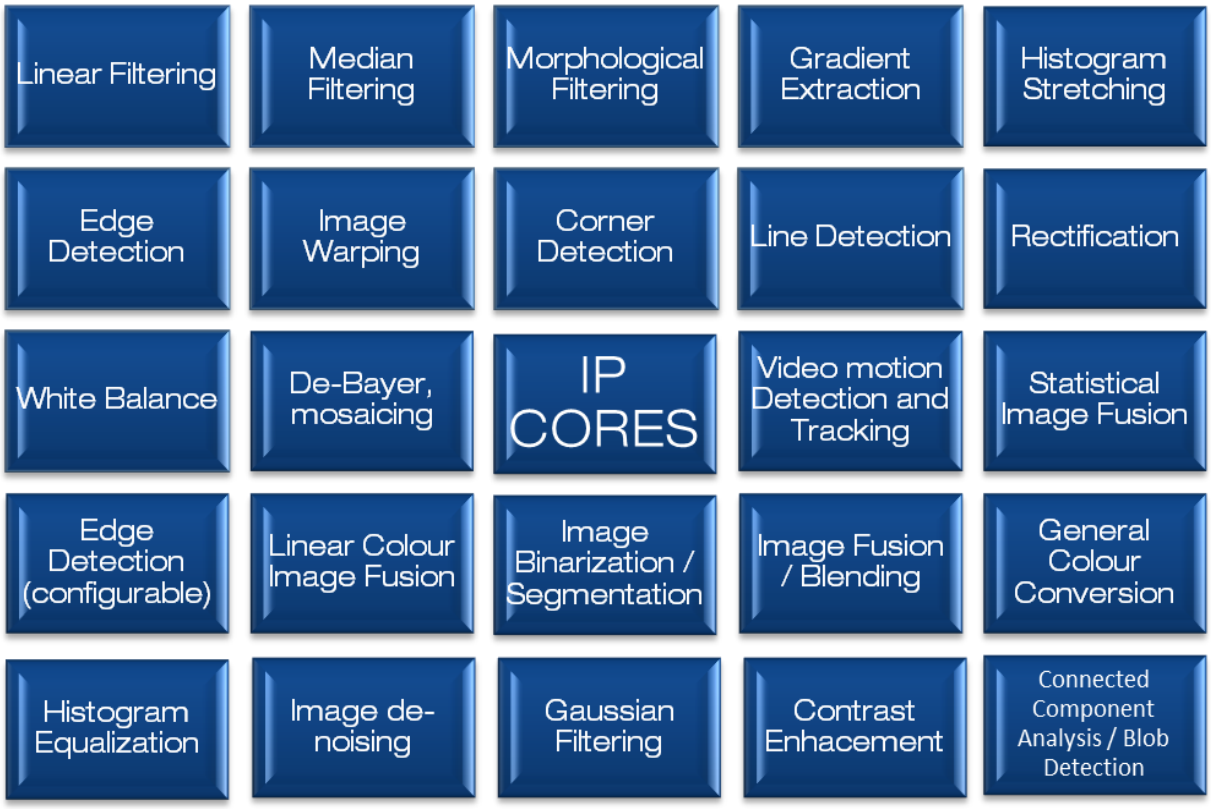
Table 2: Resolution / FPS table

IP Cores

Cameleon camera can work with One Pixel per Clock Performance IP cores only.

Key features:

- Real time performance
- Self-contained modules
- Compact configuration
- Continuous one pixel per clock performance
- High-clock rate
- Support for various FPGA Families
- Fully Pipelined Architecture
- Low-latency
- 8-bit I/O and 16-bit data path accuracy



NOTE: All IP Cores listed above are optional equipment and not included in the standard camera configuration. Implementation and integration of the standard IP Core into the camera FPGA is included in the price. Any modification is not the part of the standard service.

Mechanical drawings

Cameleon Base OEM

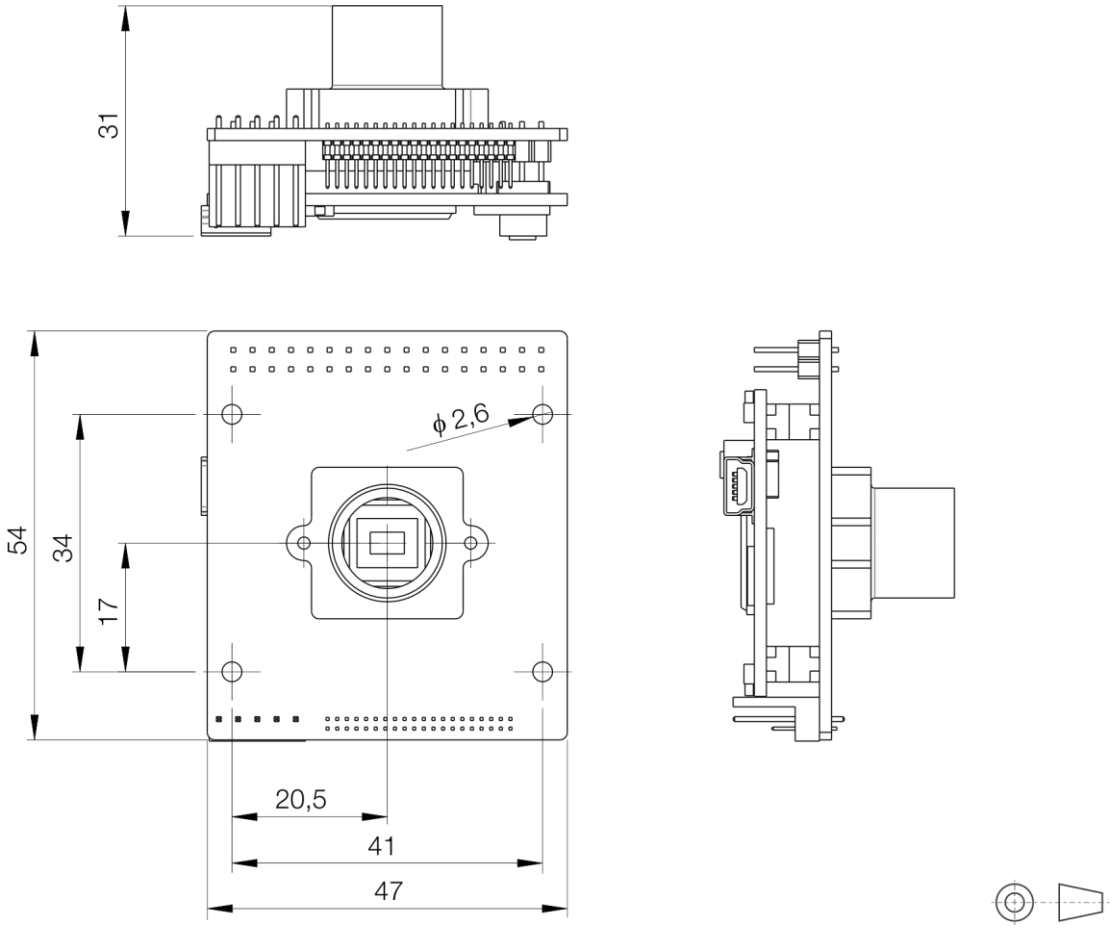


Figure 4: Cameleon Baseboard in OEM version and M12 lens holder

Cameleon Head OEM

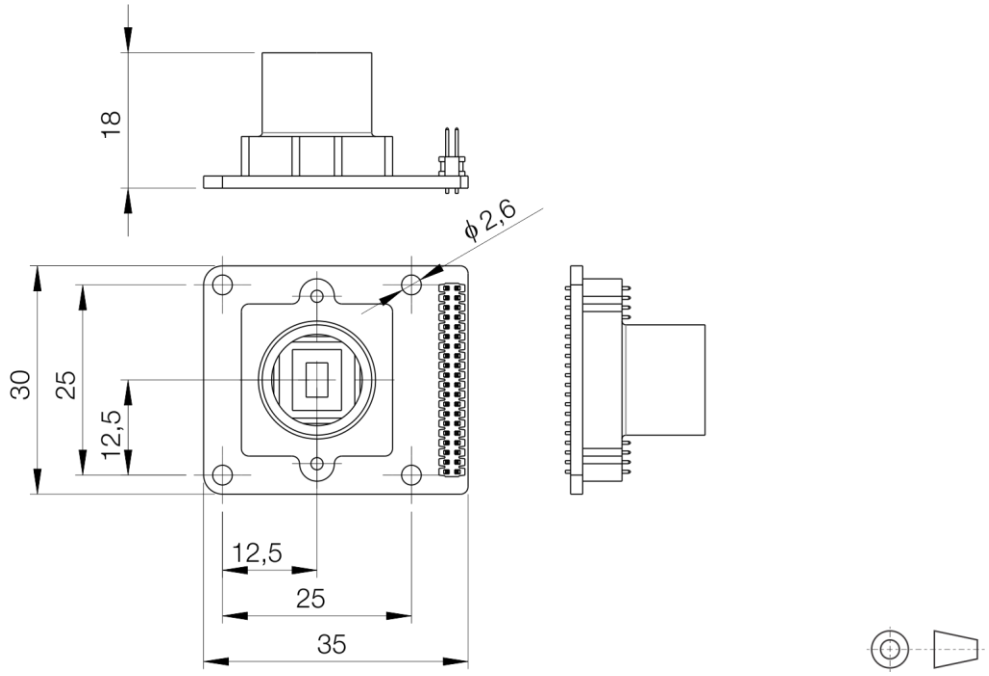


Figure 5: Cameleon Head in OEM version

Cameleon in a housing with C-mount lens holder (IP67 optional)

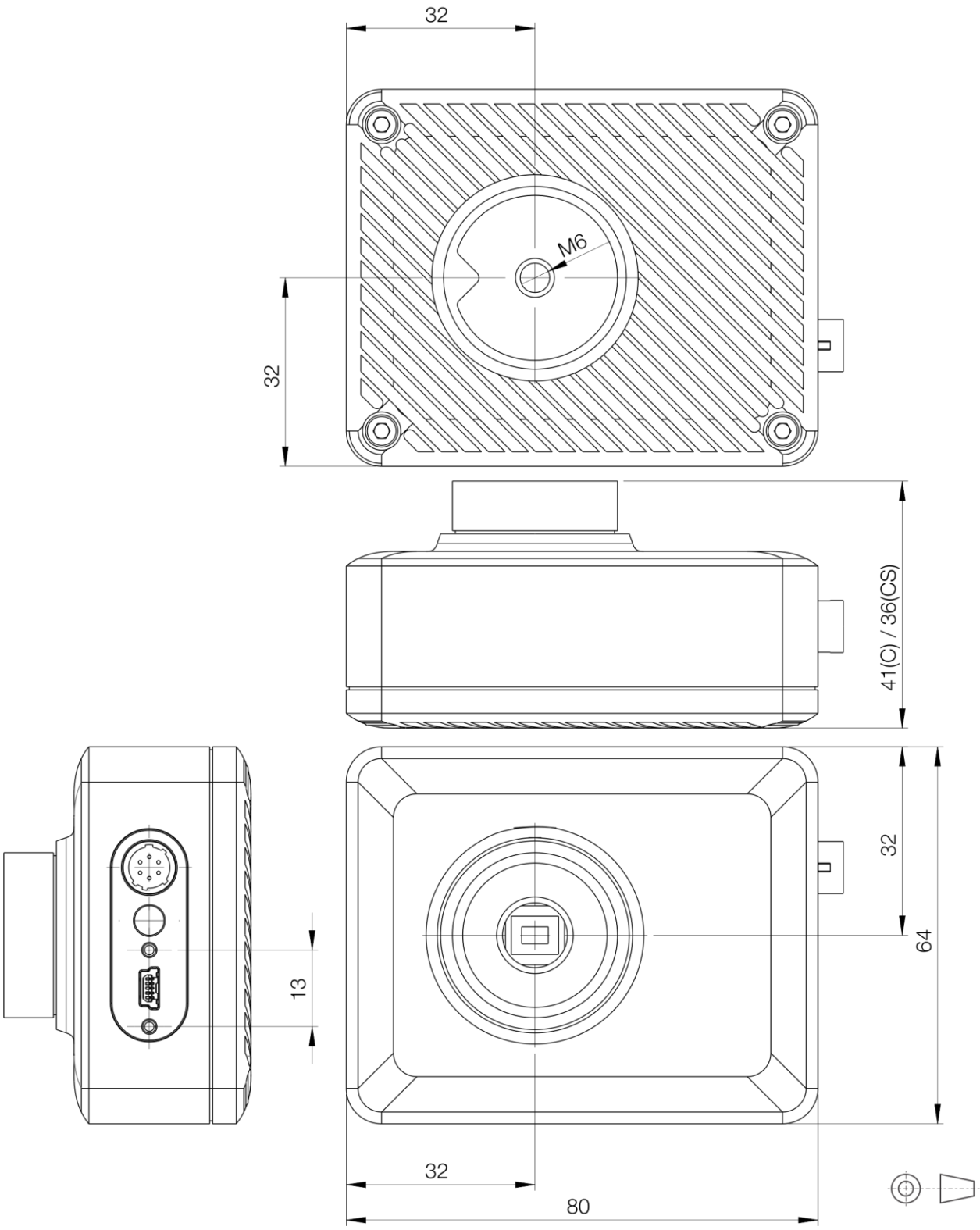


Figure 6: Cameleon in a housing with C-mount lens holder

Cameleon in a housing with LED lighting (IP67 optional)

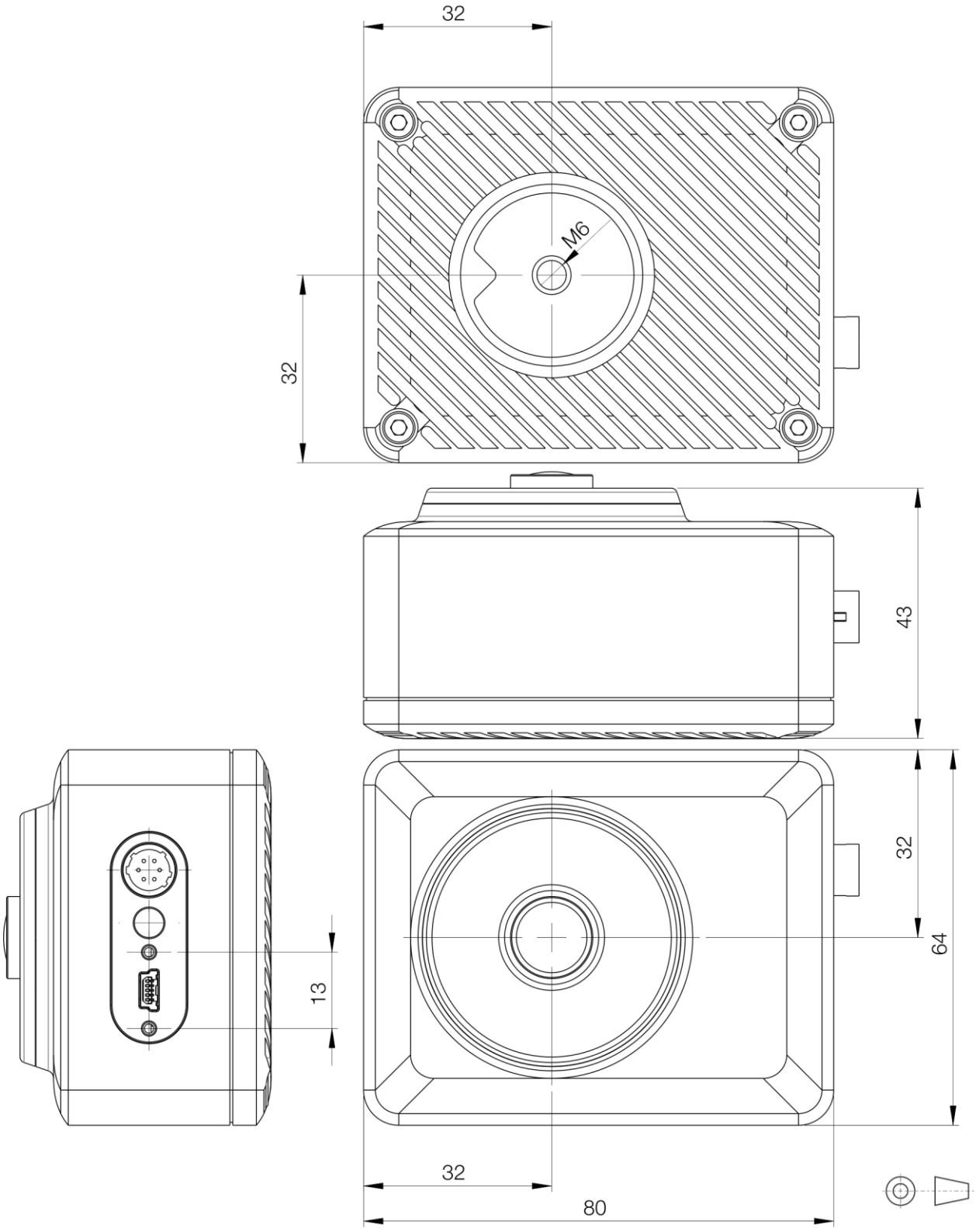


Figure 7: Cameleon in a housing with C-mount lens holder and LED-ring